

Fig. 1

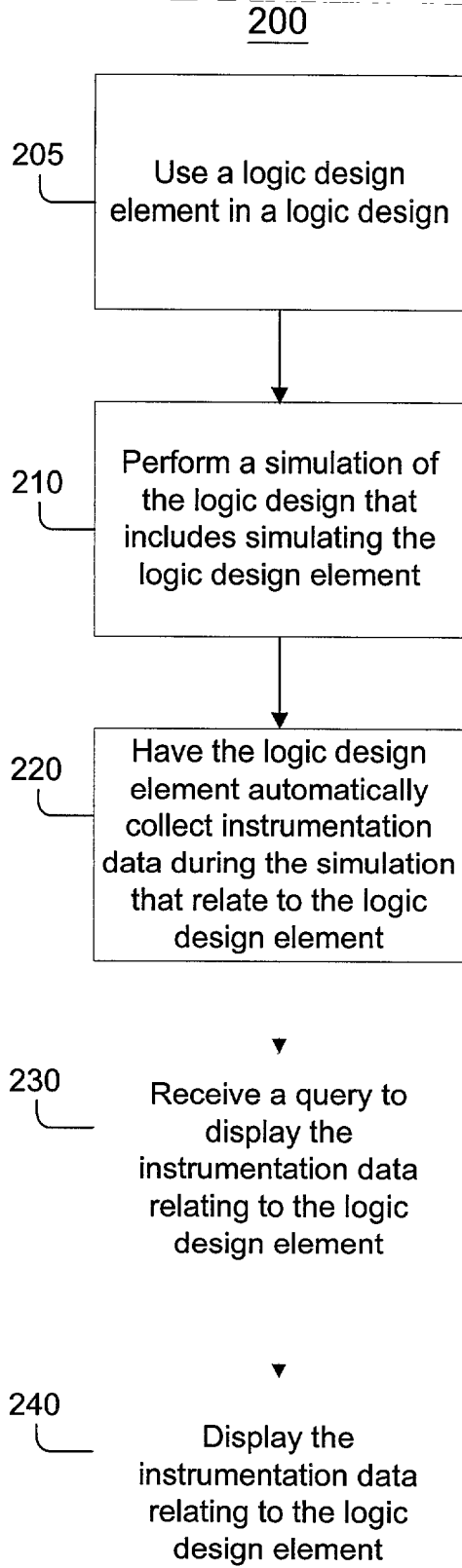


Fig. 2

300

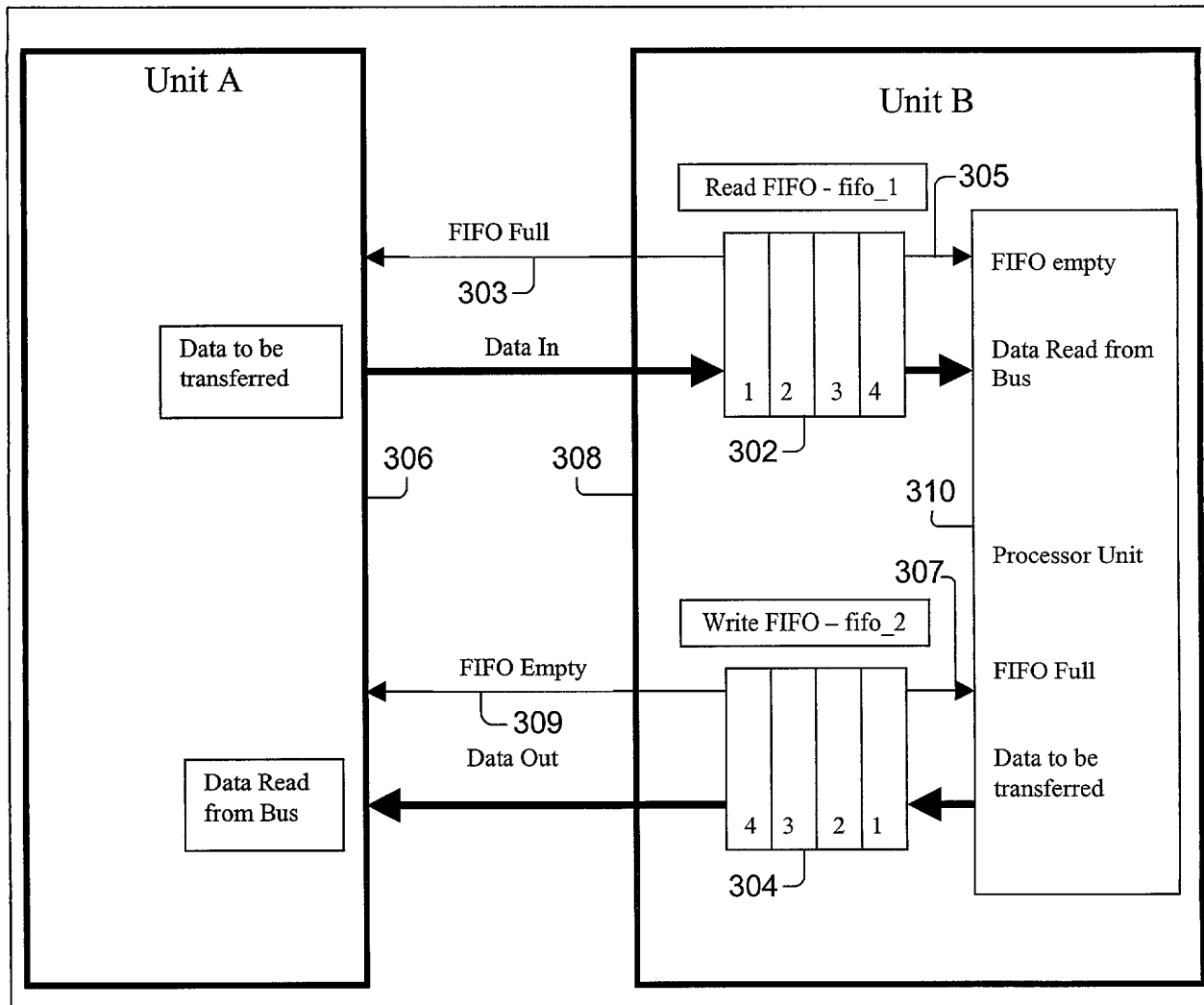


Fig. 3A

350

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DQCLK:468> ex /fifo fifo_2
FIFO fifo_2: 4 words X 32 bits (32 B); valid entries = 0; valid
enqueued entries = 4; rd_ptr = 1; wr_ptr = 1
```

sample m_distrib	234	158	52	24
percent	50%	34%	11%	5%
cumul percent	50%	84%	95%	100%
fifo entries	0	1	2	3

Fig. 3B

400

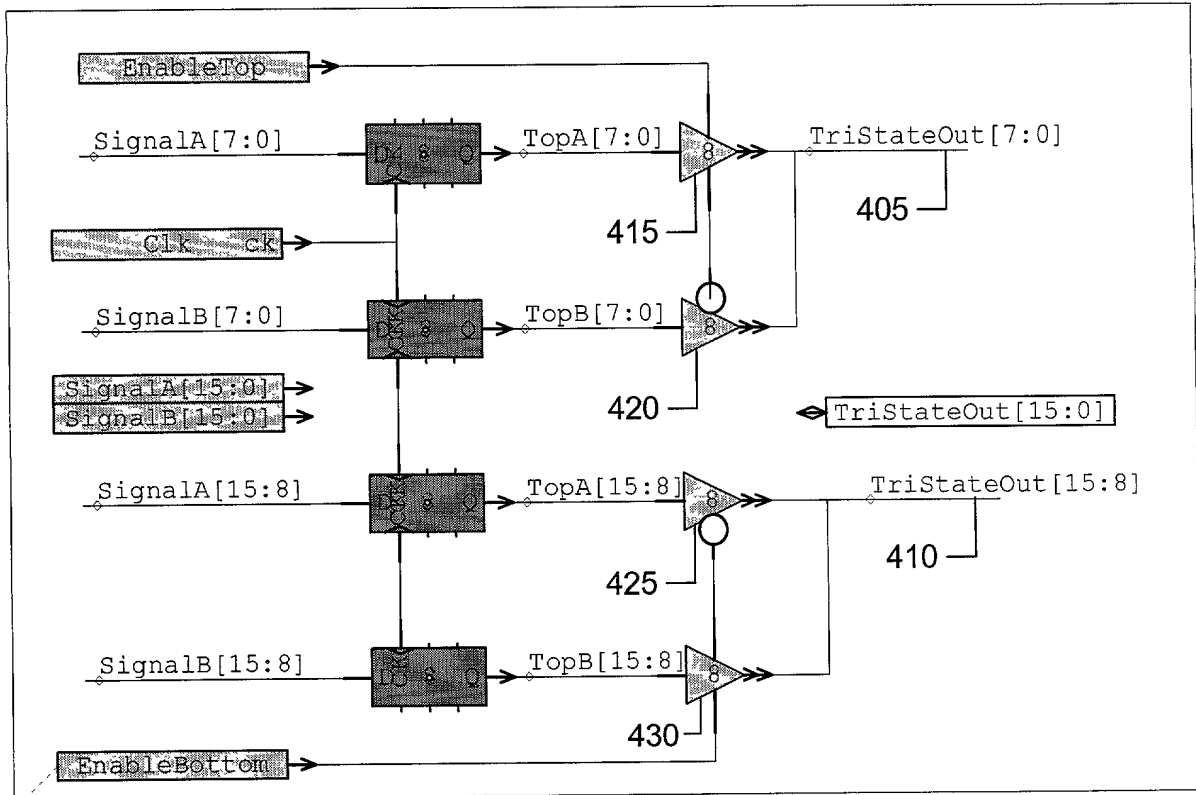


Fig. 4A

450

Driver	15	8	7	0
Undriven	0 ( 0.0%)	0 ( 0.0%)		
gate 37 TopA[15:8]	1167 ( 46.7%)			
gate 33 TopB[15:8]	1333 ( 53.3%)			
gate 28 TopB[7:0]			689 ( 27.6%)	
gate 26 TopA[7:0]			1811 ( 72.4%)	
Conflict	0 ( 0.0%)	0 ( 0.0%)		

Fig. 4B